I CLAIM:

1. A method of manufacturing an integrated circuit carrier, the method including the steps of

providing a substrate;

demarcating at least one receiving zone for an integrated circuit on the substrate and a plurality of island-defining portions arranged about said at least one receiving zone; and

creating rigidity-reducing arrangements between neighboring island-defining portions by removing material from the substrate.

2. The method of claim 1 which includes forming electrical contacts in said at least one receiving zone and forming an electrical terminal in each island-defining portion, each electrical terminal being electrically connected via a track of a circuitry layer to one of the electrical contacts.

3. The method of claim 2 which includes forming the circuitry layer on a surface of the substrate by depositing a metal layer on the substrate.

4. The method of claim 1 which includes demarcating said at least one receiving zone and the island-defining portions by means of a mask applied to a surface of the substrate.

5. The method of claim 4 which includes removing the material of the substrate to create the rigidity-reducing arrangements by etching through the substrate after exposure of the substrate, carrying the mask, to light.

6. The method of claim 1 which includes creating the secondary rigidity-reducing arrangements by etching through the substrate.

7. The method of claim 1 which includes forming the substrate from a wafer of undoped silicon having an insulating layer.

8. The method of claim 1 which includes demarcating said at least one receiving zone by forming a recess in the substrate.

9. The method of claim 8 which includes forming the recess by etching the substrate.

10. The method of claim 2 which includes demarcating said at least one receiving zone by forming a passage through the substrate, a region of the substrate surrounding the passage carrying the electrical contacts.

11. The method of claim 10 which includes forming the passage by etching the substrate.